Future Prospects for Moore's Law

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Abstract:

"Moore's law" was the first widely-recognized indicator of progress in integrated circuit technology. It fits into a broader set of metrics that are used to characterize the detailed state of semiconductor technology today and is often used loosely as a surrogate for most of them. Some of these are the logic-gate/memory-bit-level metrics of cost, operating speed, active power, and standby power. For more than four decades, all of these have been improved at exponential pace principally by scaling the feature sizes of the device structures within ICs. Today, we label successive ~0.7x overall scaling milestones as semiconductor "technology nodes." The semiconductor industry's official definition, progress tracking, and future projections for IC technology nodes are documented in the International Technology Roadmap for Semiconductors (ITRS), which is updated annually. The updates are based on a consensus-building process conducted by Technology Working Groups with approximately 1000 international participants from industry (chipmakers and their suppliers), academia, and government. The principal purpose of the ITRS is to highlight future research and development needs in support of continued IC progress. It accomplishes this primarily by creating a (rolling 15-year-horizon) strawman extrapolation of recent trends for hundreds of IC technology parameters and color-coding them in terms of estimated risk of solution based on the best-guess level of R&D effort. Examples of the technology parameter projections, risk assessments, potential solutions, and other highlights of the 2003 ITRS are presented.

Of course, the scaling-based IC technology trends, such as Moore's Law, will eventually slow from their average pace of the 40+ years. However, we are still not close enough to any obvious "ultimate limits" to predict when there will be large departures from historic rates of progress in most of the high-level metrics. In 2004, even our "hp 90-nm CMOS" technology is still fairly far from "hard" physics limits, and significant "post-CMOS" research is underway. It is also important to note that the practical limits are not "sharp cliffs" and almost always involve cost and other product-level tradeoffs. In other words, it is not likely that progress will halt just because there are no viable purely technical solutions to further scaling, but because these solutions would cost more than a particular market will support. In this regard, it is quite likely that the development and/or one-time-engineering costs will be more prohibitive than incremental manufacturing cost. This is already becoming the case for many potential low-volume products. Another complication in forecasting even ultimate CMOS, much less a potential successor, is that the significant parameters characterizing the technology don't tend to saturate simultaneously. At a particular technology node, CMOS processes are developed in several flavors, optimizing the tradeoffs between various customer care-abouts such as speed, power dissipation, on-chip integration of diverse functions, and cost. Among all of the historical IC technology trends, the most obvious saturation to date has been in chip size. For example,

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DRAMs used to quadruple bit count every three years based on nearly equal contributions from die area increase and device/area decrease. Now they are quadrupling the bits every four years with essentially no increase in die size. Thus, for DRAMs and most other ICs, growth in chip size is no longer supporting Moore's Law. However, if you were to regard thin-film-transistor flat-panel displays as "chips," you would conclude that chip area is still increasing!

Today, almost everyone agrees that we have hopeful potential solutions for practically extending general CMOS scaling to at least the "hp 32-nm node." At this node, minimum transistor gate lengths are projected to be in the 13-15 nm range, which is still within theoretical CMOS device limits. What makes people more nervous in this regime are things like affordable lithography, manufacturing control of device parameters, and interconnect resistivity. Of course, there is considerable debate about how much farther ultimate CMOS lies beyond that point and what, if anything, might take its place. Thus, each of the last few editions of the ITRS have put increased emphasis on highlighting the need for additional post-CMOS research. The Semiconductor Industry Association (SIA) is the U.S. sponsor of the ITRS and uses it as input for creating recommendations on technology strategy. Based on the 2003 ITRS and a recent ITRS gap analysis by the Semiconductor Research Corporation, the SIA has recently presented a recommendation to the President's Council of Advisors on Science and Technology for increased long-range research in nanoelectronics. In summary, the SIA believes that the IC industry faces two grand challenges worthy of very significant new federal funding: (1) scaling limits of "evolutionary lithography/thin-film manufacturing" and (2) scaling limits of "charge-transport devices/interconnect." Furthermore, the SIA suggests that these might be overcome through new and synergistic research in the under-funded broad areas of:

(1) "directed self-assembly" of complex structures with "nanoelectronics-functionality" (computation, communication, etc.) and
(2) "beyond (classical) charge transport" signal-processing/computational technology (e.g., based on quantum-states), respectively. The prospect is not necessarily for an abrupt disruption of incumbent CMOS technology, which will probably persist for a long time. A more likely scenario is the development of new technologies that will begin to complement CMOS in "hybridized nano-electronics" prior to any eventual full replacement of CMOS functionality.

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Eighth Annual High Performance Embedded Computing Workshop

Lincoln Laboratory

September 28, 2004

Robert Doering

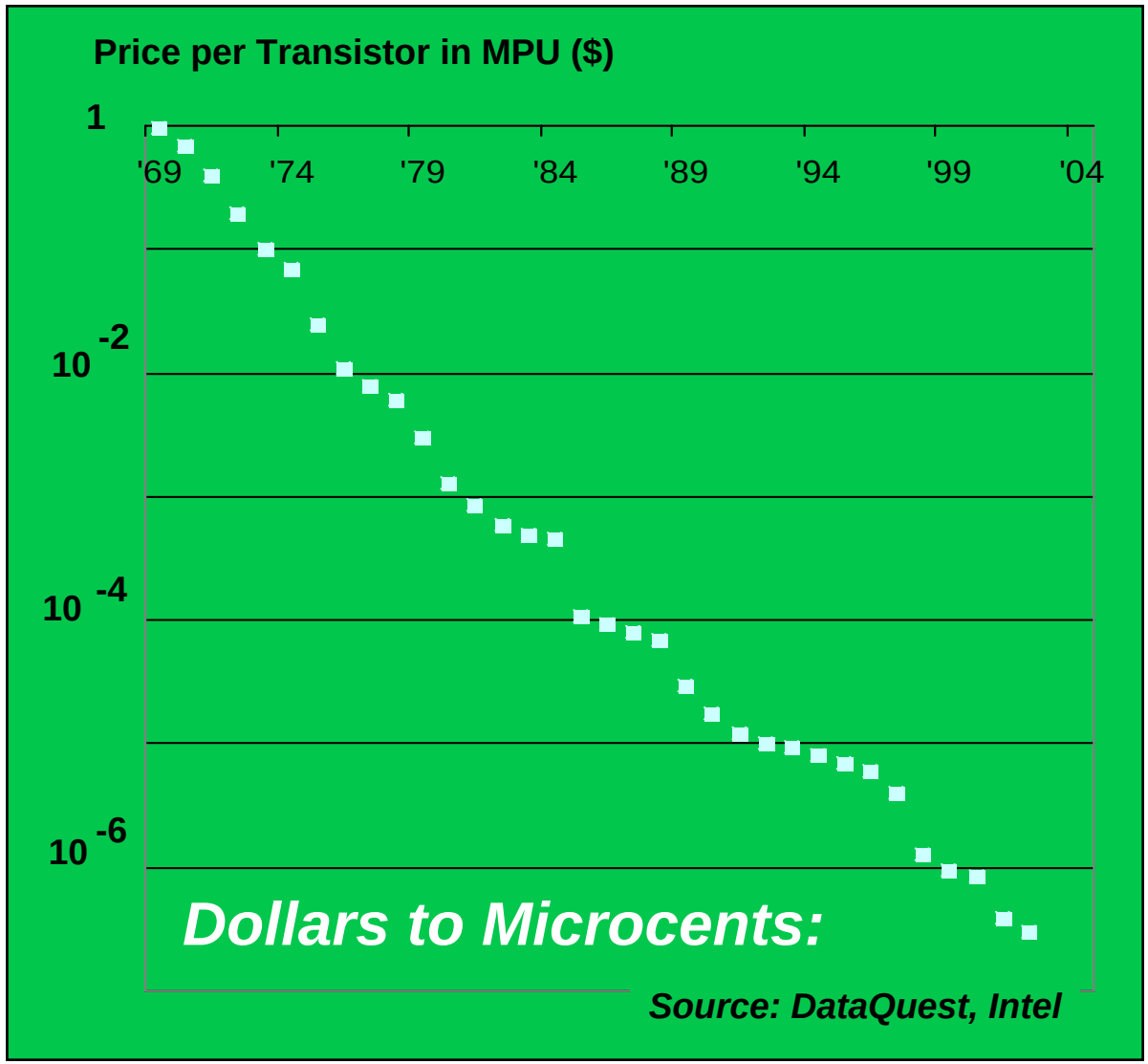
Texas Instruments, Inc.

Generalizations of Moore's Law

Exponential trends in:

- More functions* per chip
- Increased performance
- Reduced energy per operation
- Decreased cost per function (*the principal driver*)

* *transistors, bits, etc.*



High-Level CMOS Technology Metrics – What are the Limits ?

- **Component Diversity** (integrated logic, memory, analog, RF, …)
- **Cost/Component** (e.g., μ¢/gate or μ¢/bit in an IC)
- **Component Density** (e.g., gates/cm^2 or bits/cm^2)
- **Logic Gate Delay** (time for a gate to switch logic states)
- **Energy Efficiency** (energy/switch and energy/time)
- **Mfg. Cycle Time** (determines time-to-market for new designs as well as rate of yield learning)

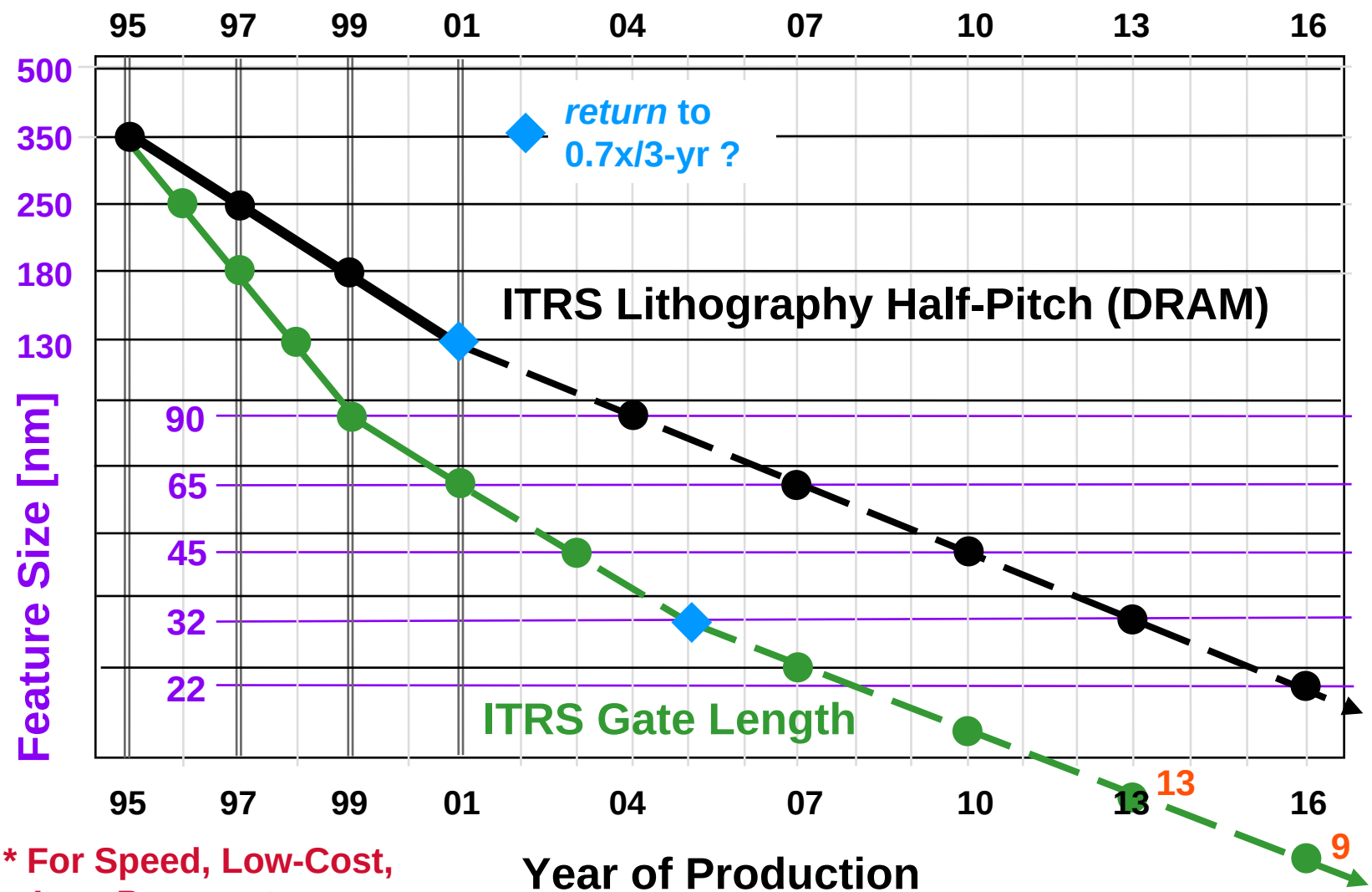
All of these are limited by multiple factors inter-linked into a complex "tradeoff space." We can only touch on a few of the issues today !

State-of-the-Art CMOS in 2004

- **ITRS Technology Node:** **90 nm** (half-pitch of DRAM metal lines)
- **4T-Gates/cm^2:** **37x10^6** (150 million transistors/cm^2)
- **6T-eSRAM bits/cm^2:** **10^8** (600 million transistors/cm^2)
- **Cost/Gate (4T):** **40 µ¢** (high volume; chip area = 1 cm^2)
- **Cost/eSRAM bit:** **10 µ¢** (high volume; chip area = 1 cm^2)
- **Gate Delay** **24 ps *** (for 2-input, F.O. = 3 NAND)
- **Switching Energy** **0.5 fJ *** (for inverter, half-cycle)
- **Passive Power** **6 nW *** (per minimum-size transistor)
- ***Min.* Mfg. Cycle Time** **10 days** (or 3 mask levels/day)

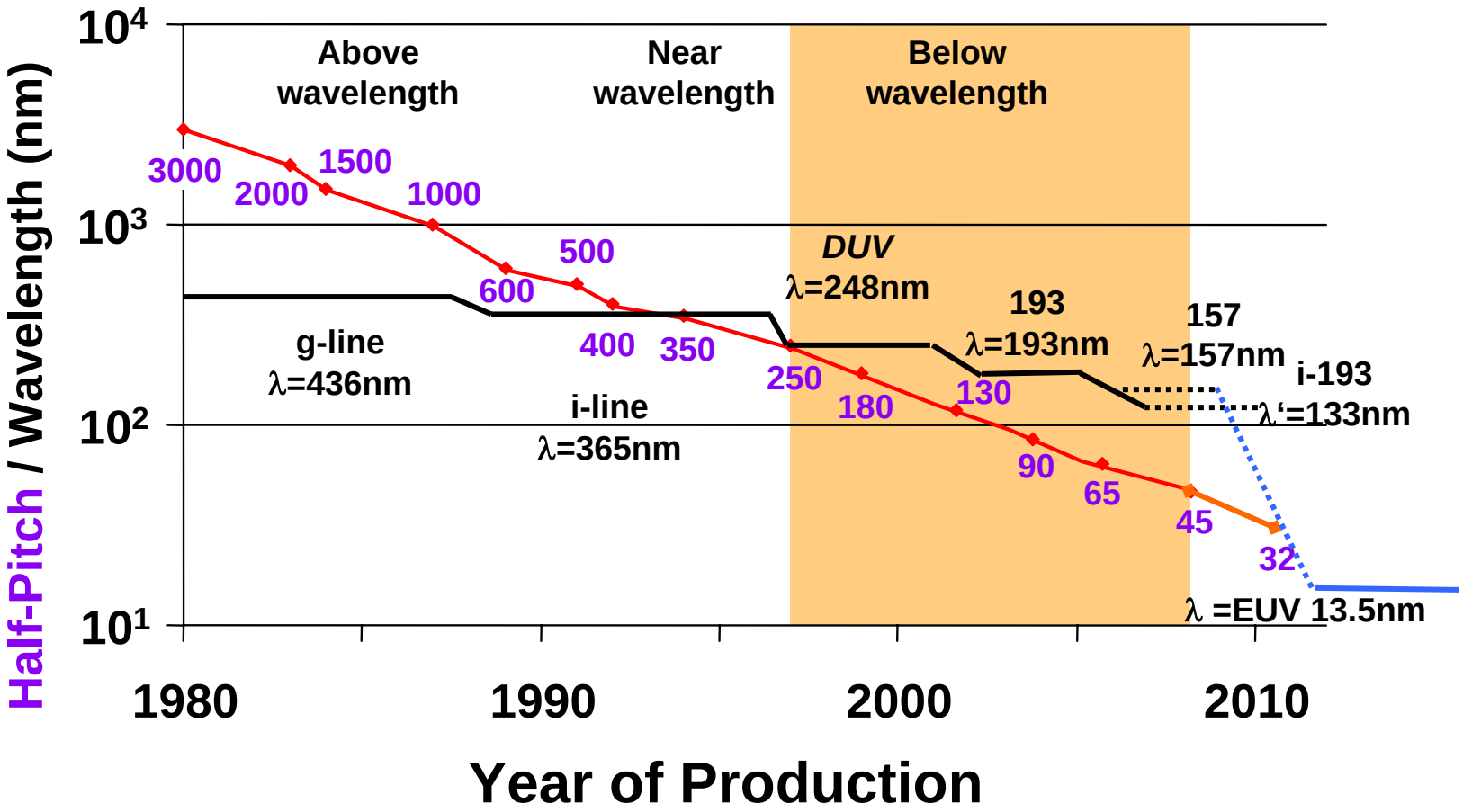
*** Values at extreme tradeoff for MPU application**

Scaling -- Traditional Enabler of Moore's Law*



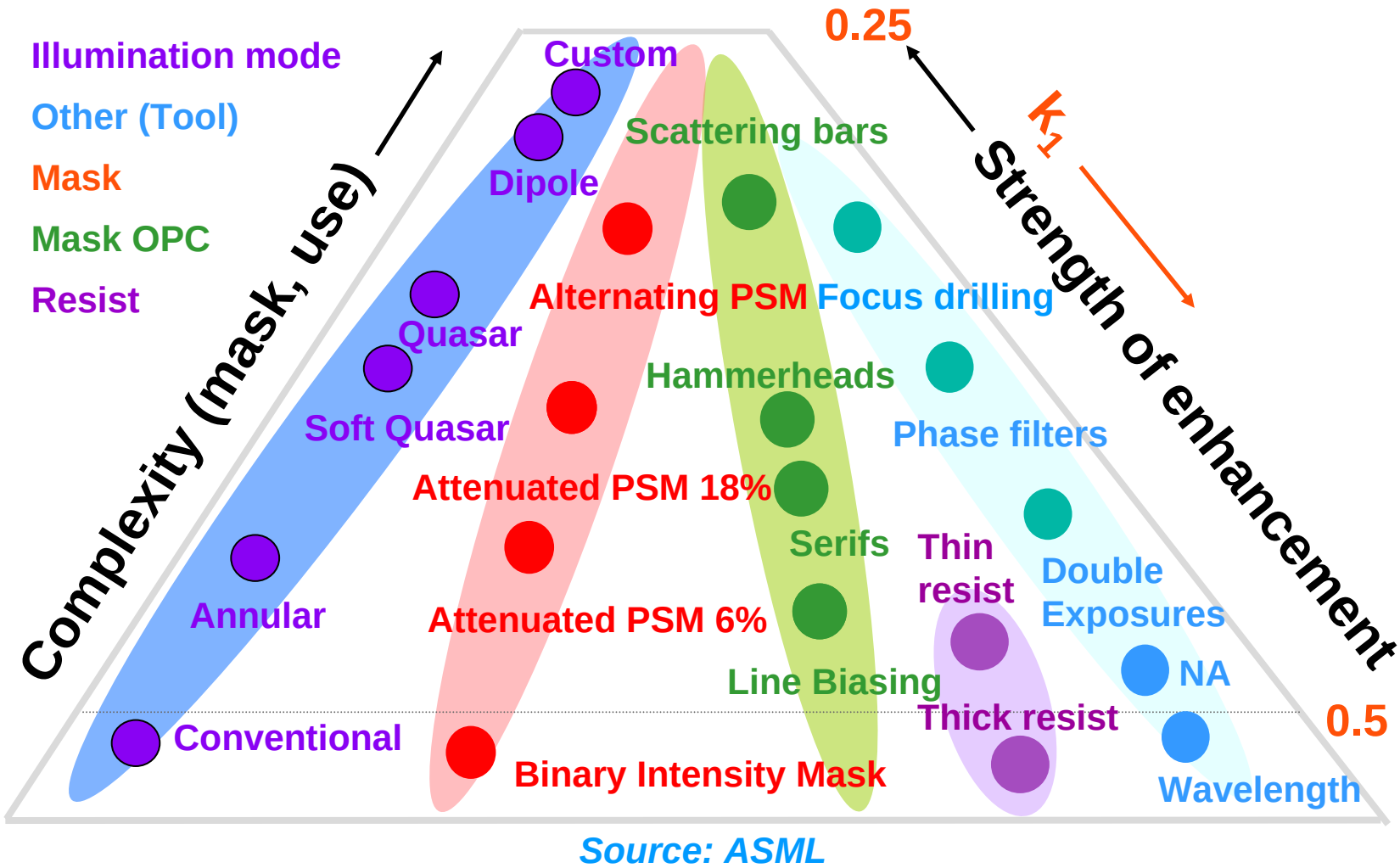
* For Speed, Low-Cost, Low-Power, etc.

Can We Extend the Recent 0.7x/2-year Litho Scaling Trend ?



For lithography, it's a question of cost and control/parametric-yield !

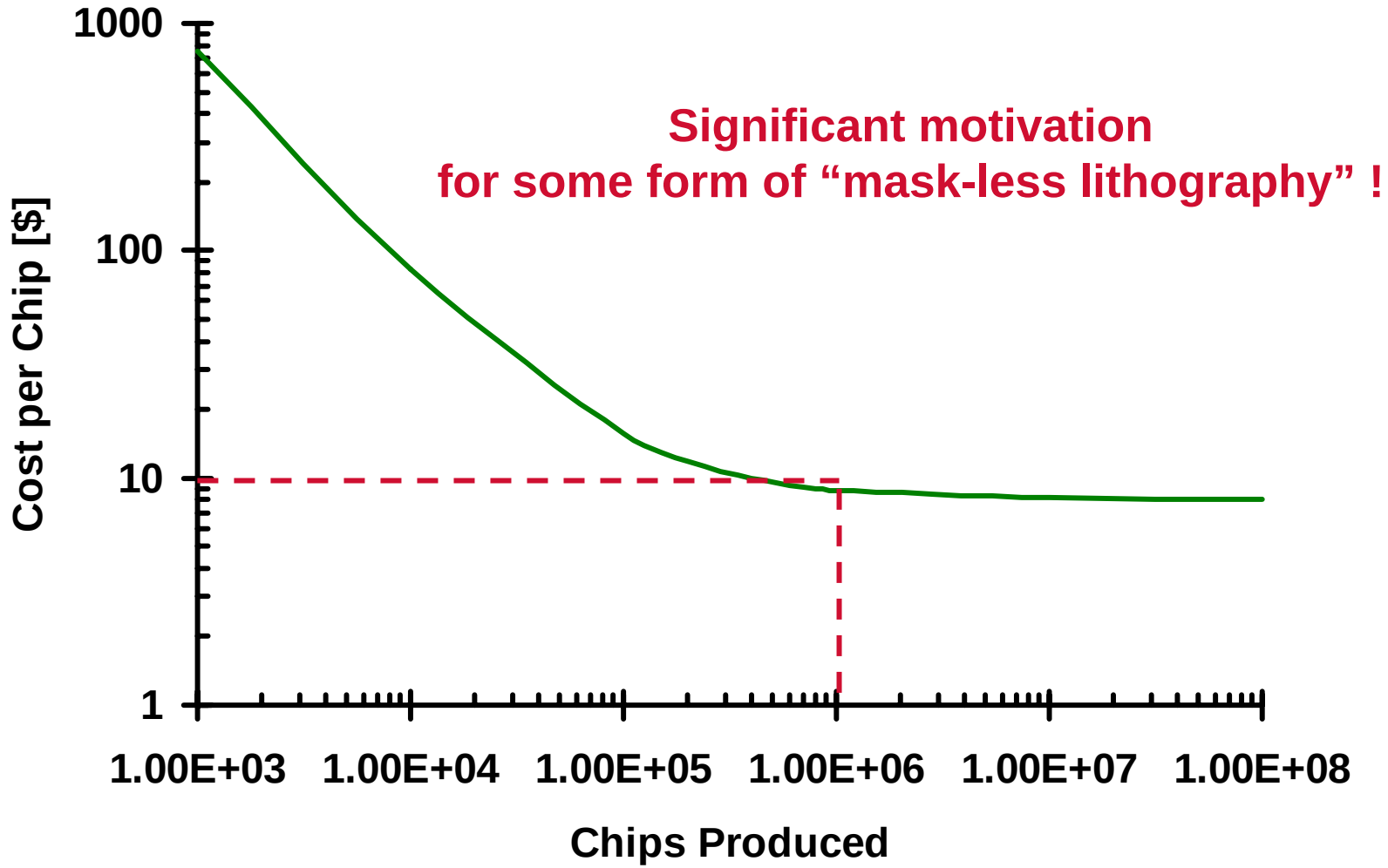
A "Bag of Tricks" for Optical-Extension



Source: ASML

Of course : increasing complexity → increasing cost !

Amortization of Mask Cost @ 130nm

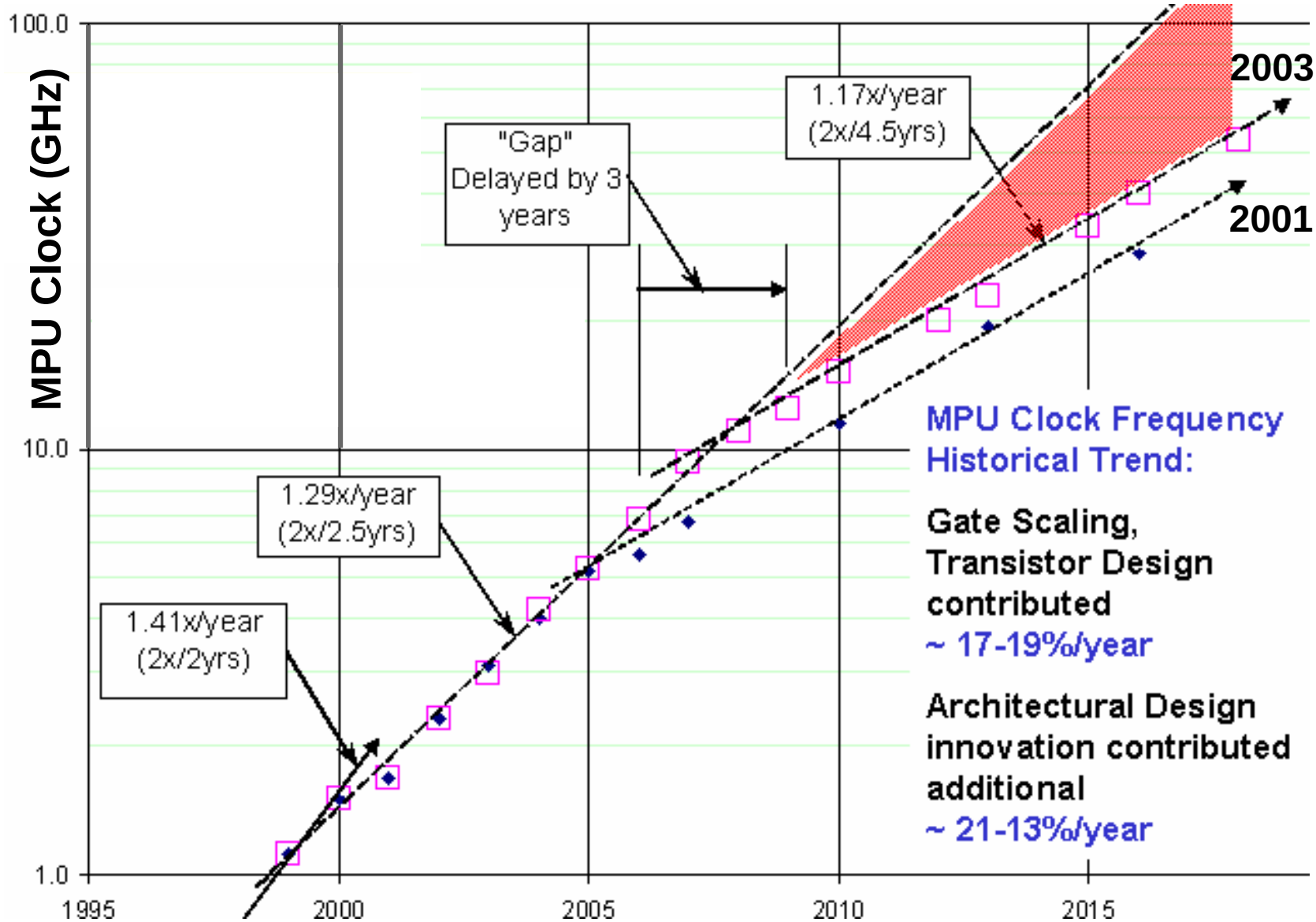


~ 1 million units required to get within 10% of asymptotic cost !
(and getting worse with continued scaling)

Of course, overall scaling is limited by more than just lithography !

- **Growing Significance of Non-Ideal Device-Scaling Effects:**
  - **I_{ON} vs. I_{OFF} tradeoff**
  - **unfavorable ρ and L scaling for interconnects**
- **Approaching Limits of Materials Properties**
  - **Heat removal and temperature tolerance**
  - **C_{MAX} vs. leakage tradeoff for gate dielectric**
  - **C_{MIN} vs. mechanical-integrity tradeoff for inter-metal dielectric**
- **Increases in Manufacturing Complexity/Control Requirements**
  - **cost and yield of increasingly complex process flows**
  - **metrology and control of L_{GATE}, T_{OX}, doping, etc.**
- **Affordability of R&D Costs**
  - **development of more complex and "near cliff" technologies**
  - **design of more complex circuits with "less ideal" elements**

ITRS Tries to Address Top-Down Goals

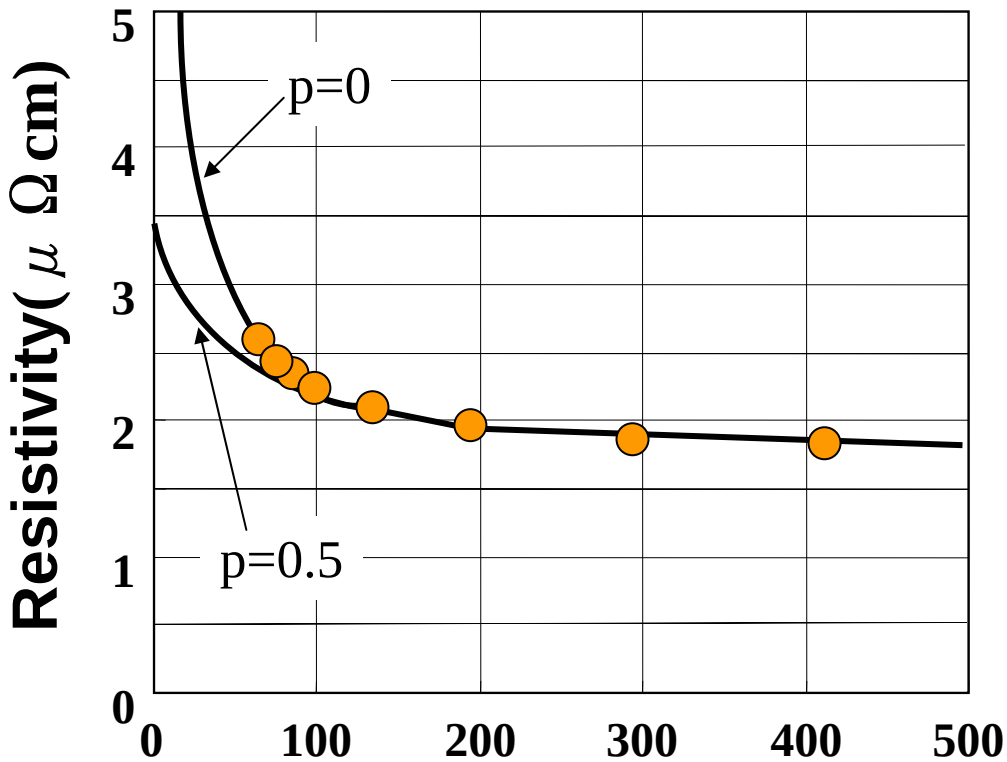


ITRS Highlights Scaling Barriers, e.g.:

Production Year:	2001	2004	2007	2010	2013	2016
Litho Half-Pitch [nm]:	130	90	65	45	32	22
Overlay Control [nm]:	45	32	23	18	13	9
Gate Length [nm]:	65	37	25	18	13	9
CD Control [nm]:	6.3	3.3*	2.2	1.6	1.2	0.8
T_{OX} (equivalent) [nm]:	1.3-1.6	1.2	0.9	0.7	0.6	0.5
I_{GATE} (L_{MIN}) [µA/µm]:	-	0.17	0.23	0.33	1	1.67
I_{ON} (NMOS) [µA/µm]:	900	1110	1510	1900	2050	2400
I_{OFF} (NMOS) [µA/µm]:	0.01	0.05	0.07	0.1	0.3	0.5
Interconnect K_{EFF}:	-	3.1-3.6	2.7-3.0	2.3-2.6	2.0-2.4	<2.0

Another Interconnect-Scaling Issue

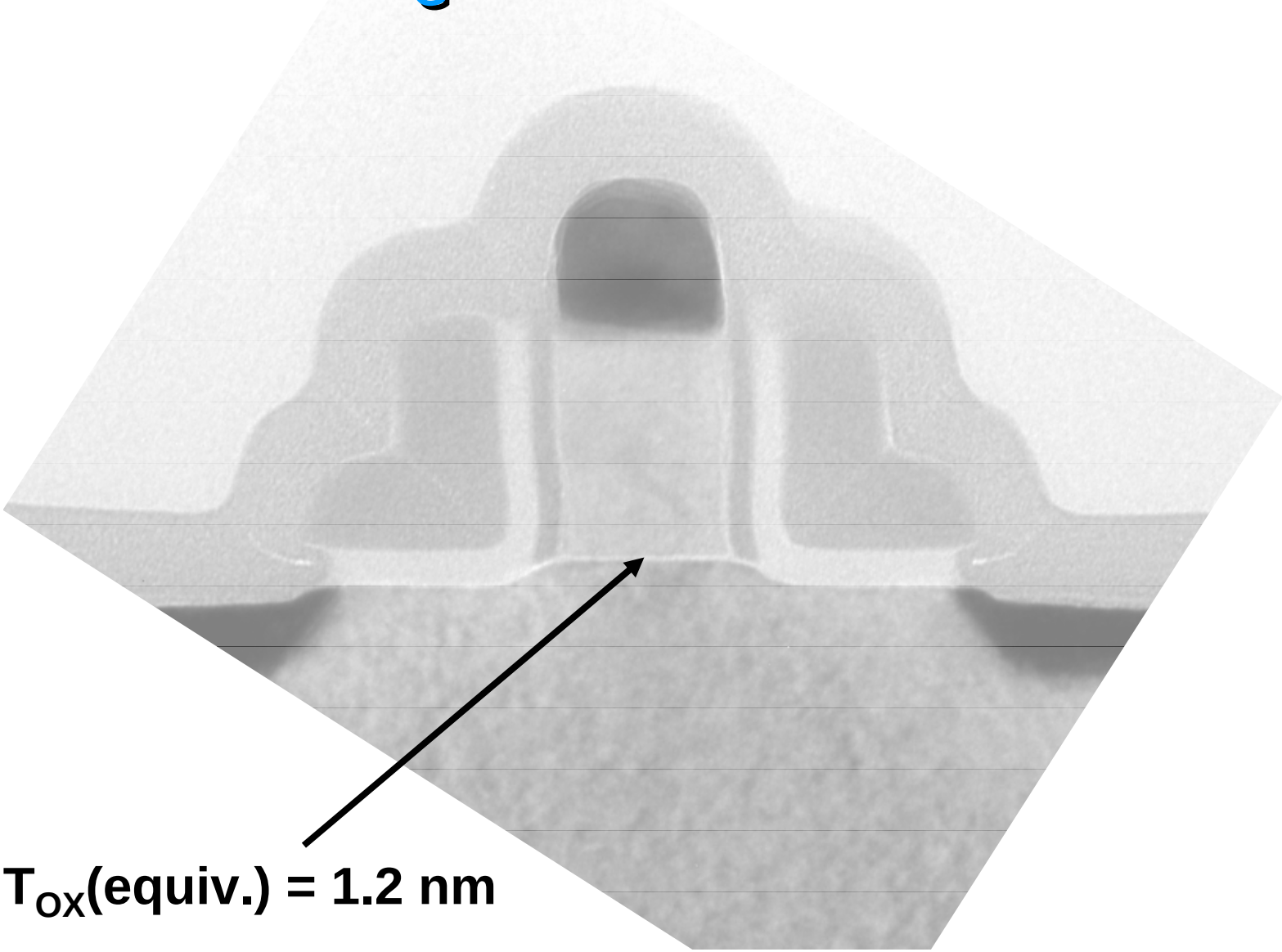
Wire width < mean-free-path of electrons



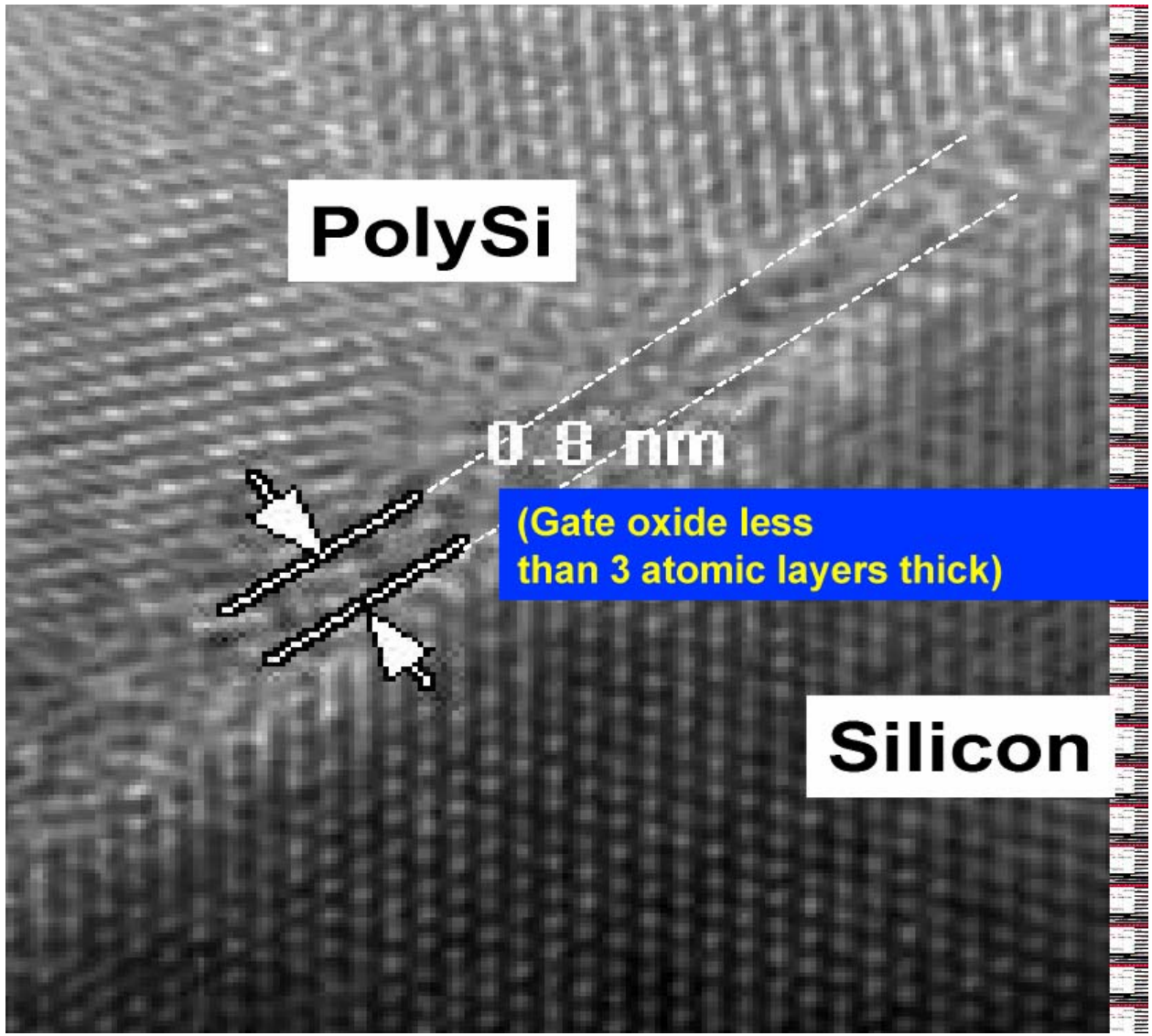
Surface scattering becomes dominant

p=0 (diffuse scattering)
p=1 (specular scattering)

2004 L_G = 37-nm Transistor



Can Some Hi-K Dielectric Replace SiON ?



Sub-nm SiON:

- **mobility**
- **uniformity**
- **leakage**

Source: Intel

In general, continued transistor scaling requires new materials, processes, …

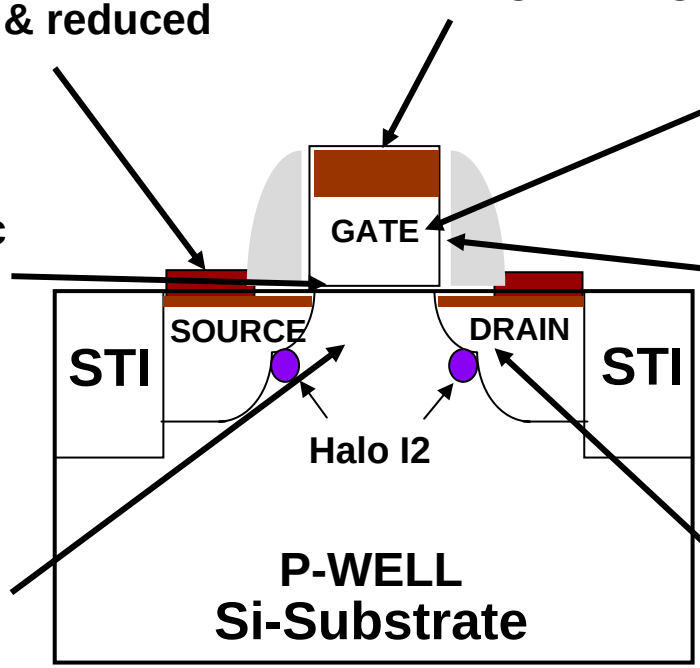
Selective-epi raised source/drain for shallow junctions & reduced short-channel effects

Ni-silicide process for low resistance at short gate lengths (near term)

Metal gate electrode to reduce gate depletion

High-κ gate dielectric for reducing gate current with thin Tox

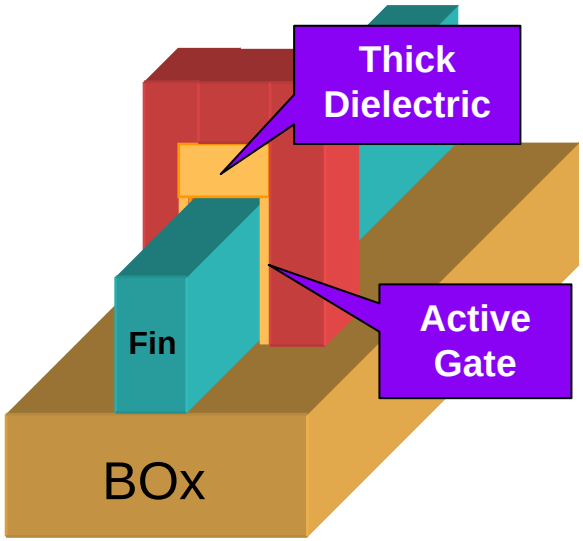
Etches for new materials that achieve profile, CD control, and selectivity



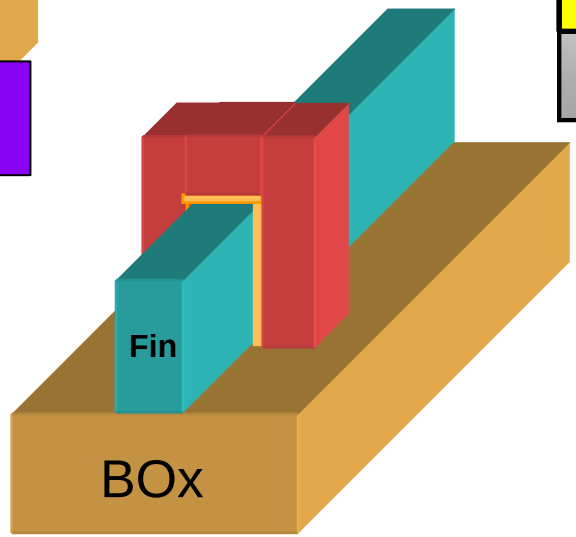
Strained channel for improved mobility

Doping and annealing techniques for shallow abrupt junctions

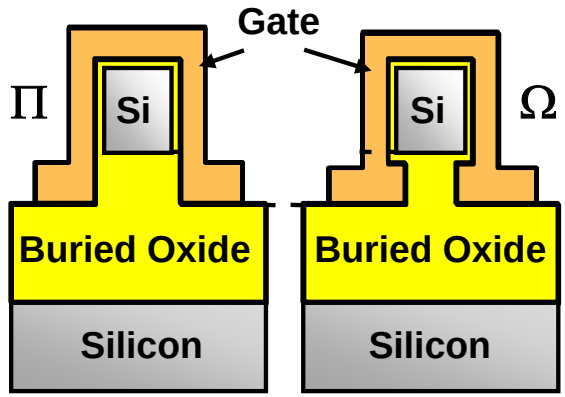
… and, eventually new structures

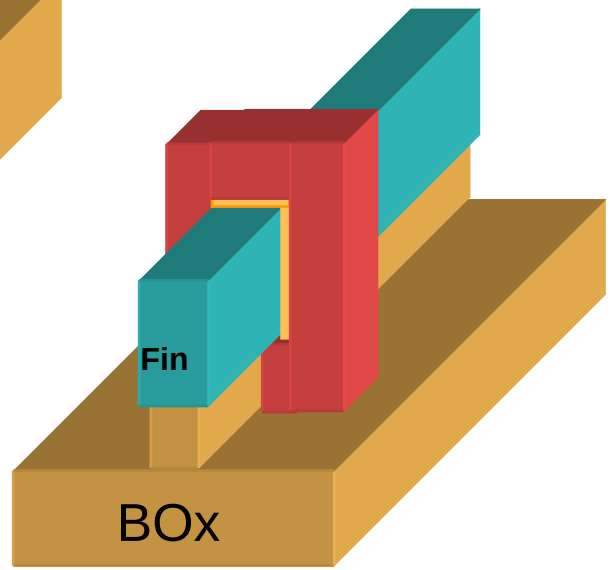


FinFET
2 Gates



Tri-Gate FET
3 Gates

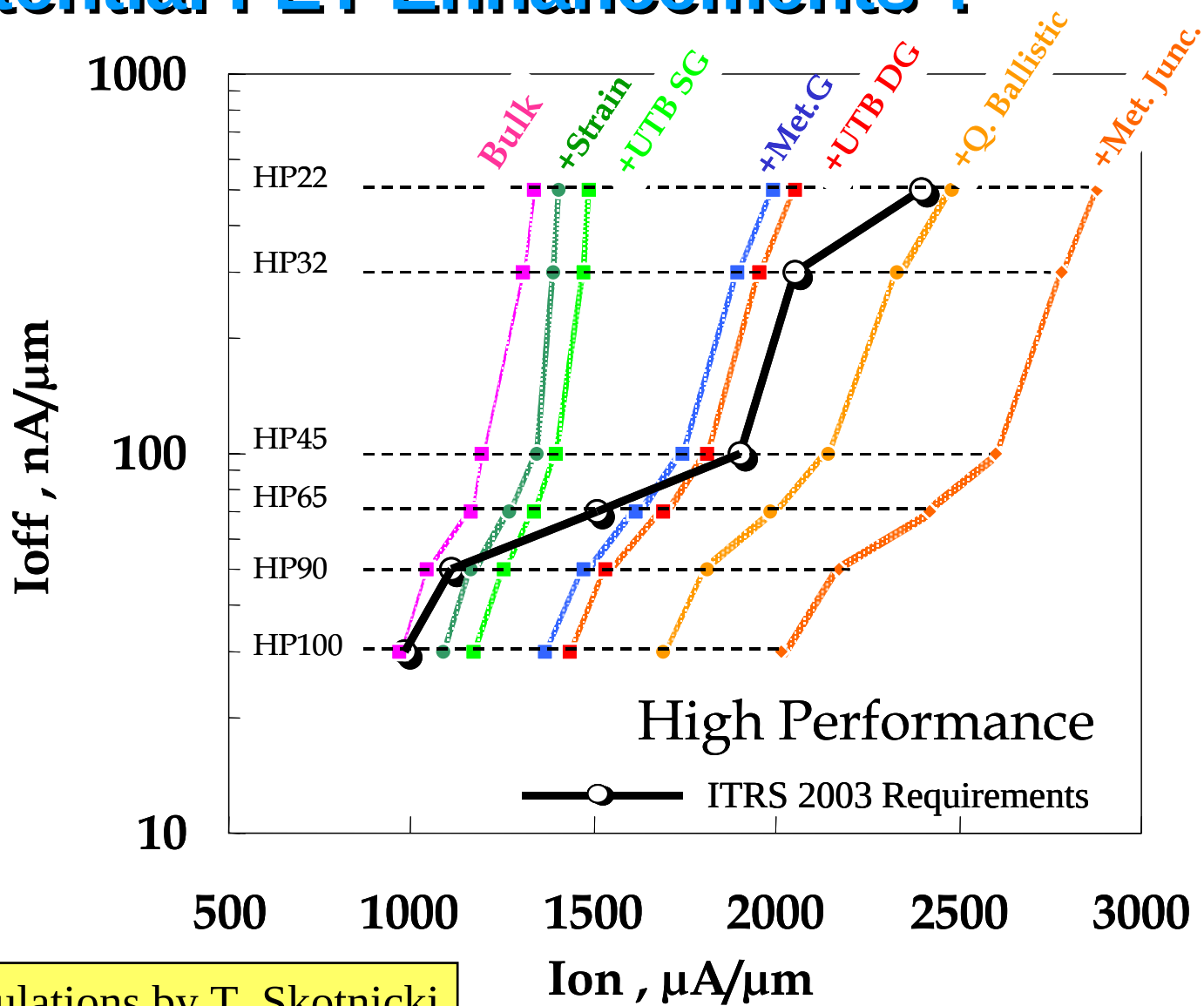




Π / Ω Gate FET
3+ Gates

Steps toward ideal “coax gate” →

Potential FET Enhancements ?



Calculations by T. Skotnicki

At PQE 2004, Professor Mark Lundstrom expressed the outlook:

"Sub-10nm MOSFETs will operate, but …

- on-currents will be ~0.5x$I_{ballistic}$, off-currents high,
- 2D electrostatics will be hard to control,
- parasitic resistance will degrade performance,
- device to device variations will be large,

and

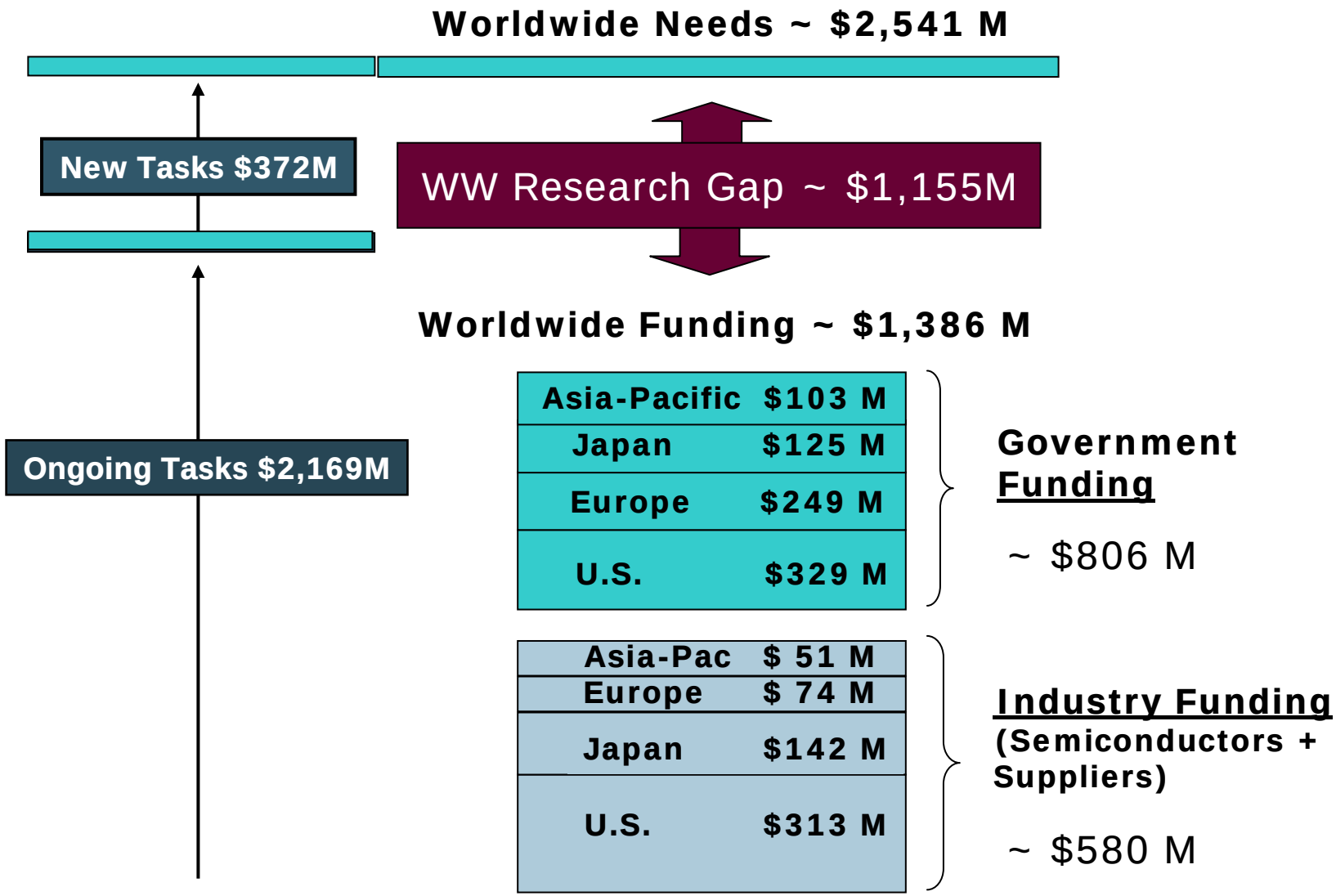
- ultra-thin bodies and hyper-abrupt junctions will be essential"

ITRS Assessment of Some Current Ideas for Successors to CMOS Transistors

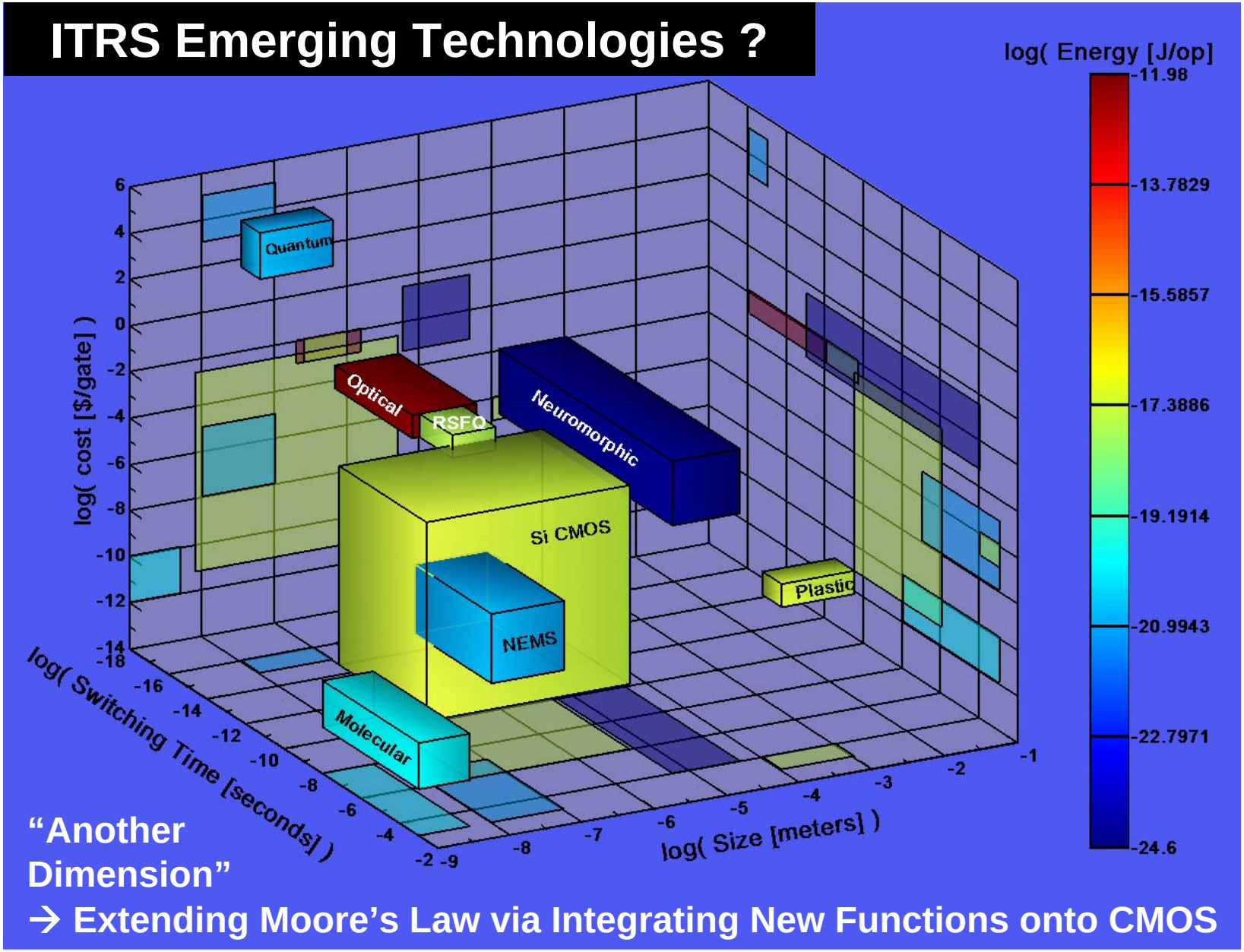
Logic Device Technologies	*Performance*	*Architecture compatible*	*Stability and reliability*	*CMOS compatible*	*Operate temp*	*Energy efficiency*	*Sensitivity Δ(parameter)*	*Scalability*
1D Structures	2.3/2.2	2.2/2.9	1.9/1.2	2.3/2.4	2.9/2.9	2.6/2.1	2.6/2.1	2.3/1.6
RSFQ Devices	2.7/3.0	1.9/2.7	2.2/2.8	1.6/2.2	1.1/2.7	1.6/2.3	1.9/2.8	1.0/2.1
Resonant Tunneling Devices	2.6/2.0	2.1/2.2	2.0/1.4	2.3/2.2	2.2/2.4	2.4/2.1	1.4/1.4	2.0/2.0
Molecular Devices	1.7/1.3	1.8/1.4	1.6/1.4	2.0/1.6	2.3/2.4	2.6/1.3	2.0/1.4	2.6/1.3
Spin Transistor	2.2/1.7	1.7/1.6	1.7/1.7	1.9/1.4	1.6/2.0	2.3/2.1	1.4/1.7	2.0/1.4
SETs	1.1/1.2	1.7/1.2	1.3/1.1	2.1/1.4	1.2/1.8	2.6/2.0	1.0/1.0	2.1/1.7
QCA Devices	1.4/1.3	1.2/1.1	1.7/1.8	1.4/1.6	1.2/1.4	2.4/1.7	1.6/1.1	2.0/1.4

No obvious candidates yet for a CMOS replacement !

SRC Research Gap Analysis (for <50nm)



ITRS Emerging Technologies ?

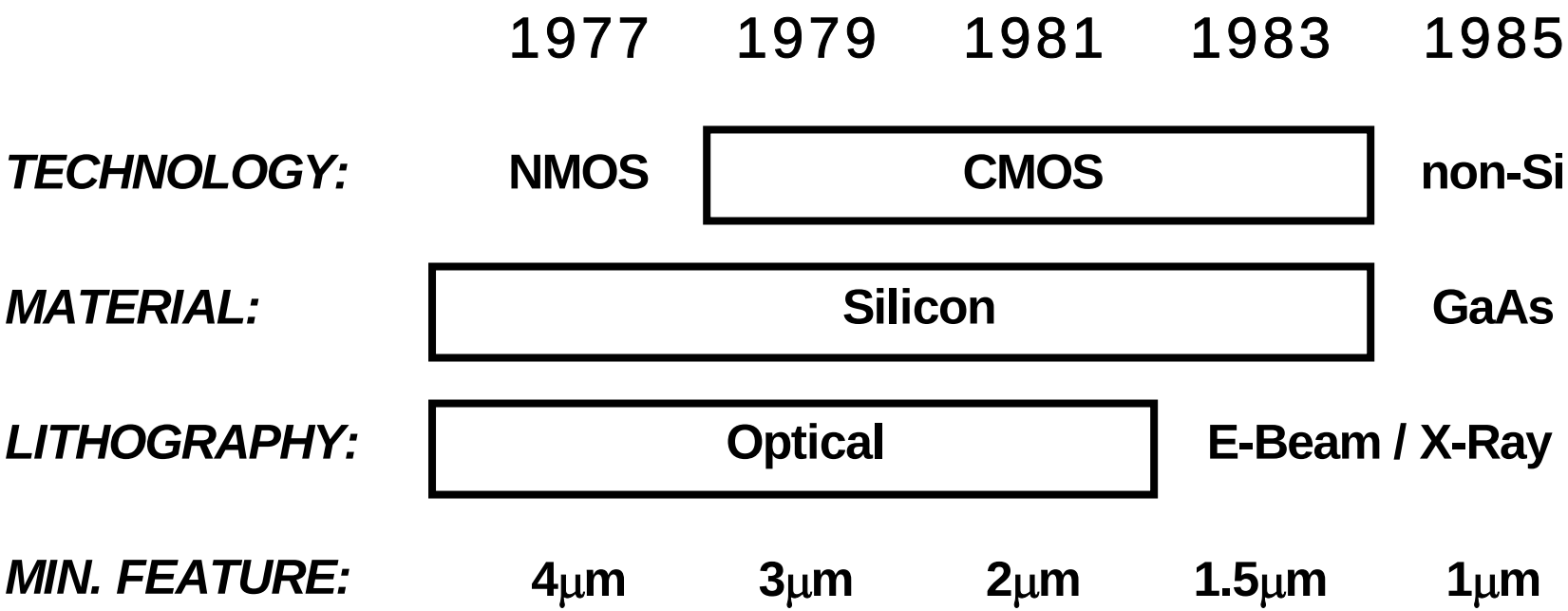


"Another Dimension"

→ Extending Moore's Law via Integrating New Functions onto CMOS

Why "Moore's Law" Is Still a Fun Topic !

A 1975 IC Technology Roadmap



What makes us think that we can forecast more than ~5 years of future IC technology any better today ?!!